

Alfa TOSCA meeting

Summary of Activities 2003-2004

Facultad de Ingeniería
Universidad Nacional de La Plata
LEICI
LABORATORIO DE ELECTRÓNICA INDUSTRIAL,
CONTROL E INSTRUMENTACIÓN

July 10, 2004

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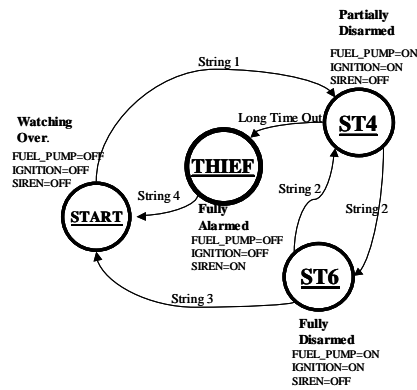
Activities during 2003

- One fellow from UNLP spent 6 months at TIMA
 - Javier Mochnacs, Electrical Engineer from UNLP and PhD candidate for UIB
 - Work performed on criticality of transient bit-flip faults in real life applications
 - Case study: Microprocessor based car Alarm

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Application to car immobilizer



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Fault Injection environments

- *The main novelty of this experiment is the fact that the external inputs (corresponding to keyboard sequences) are taken into account, simulating the functions of the studied application in a way close to the real life operation*
 - *It is important to note that in most of previous work published in this area, programs were limited to simple benchmarks bounded in time and processing fixed data (without interaction with external environment).*

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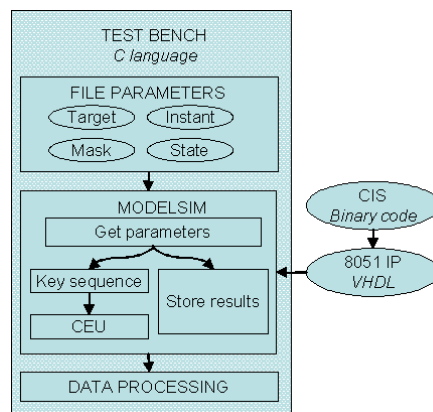
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- To perform fault injection sessions on the CIS we have simulated the 8051 microcontroller by means of a VHDL free available description.
- The C-language program describing the CIS operation was the main input of MODELSIM tool used to run fault injection experiments.
- The other inputs are the instant of occurrence of the injected bit-flip, the target memory cell and the state of the finite state machine.

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Using a Testbench to inject bit-flip faults in a VHDL description of an IP



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Experimental Results

When injecting a fault, the following situations were identified:

- no effects
- good number of outputs but wrong values
- additional undesired outputs.
- In the last two cases, the disfunction provoked by the injected fault will be considered critic only when the FSM is in state ST6, where the alarm is totally disarmed, and the outputs corresponding to *ignition* and *fuel pump* are both disabled. This is obviously the only case in which a potential cause of accident may occur.

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- A session where 824 bit-flips were injected provided the following results:
 - 723 effectless faults,
 - 33 critical faults
 - 78 faults having effects without consequences from a safety point of view (led blinking, activation of the buzzer or of the siren when the car is running).
- As stated before, fault targets, FSM state when the fault occurs, and occurrence instants were all pseudo-randomly selected to simulate the behaviour of the test vehicle in a way as close as possible of a real situation (i.e. faults due to the impact of an atmospheric neutron).

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- The analysis of experimental results shows that all critical faults occurred when the CIS finite state machine was in state ST6.
 - This is not surprising because this state is the only one where the car is running and thus, an intempetive stop either of fuel or ignition may obviously provoke an accident.
- The repartition of faults according to the perturbed memory cell are:
 - 1 fault affecting the program counter,
 - 4 corrupting one of the 21 general purpose registers,
 - the remaining 28 faults being injected in scratchpad internal memory area (96 bytes) were variables of the CIS program are stored and processed.

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Conclusions for 2003

- Experimental results obtained from bit-flip fault injection sessions performed in a purely software approach.
- An IP in VHDL of the target circuit, a 8051 microcontroller was used to simulate the behaviour of an embedded application controlling the immobilization of a car in case of theft.
- Results revealed a low but not neglictible rate of critical faults. Indeed about 4% of injected bit-flips were identified as having consequences at the safaty level
- **Publication: LATW04**, R. Velazco, J. Mochnacs, P. Peronnard, O. Calvo-
Analysis of the criticity of transient bit-flip faults in a massive embedded application†

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Activities for 2004

- Marcelo Capelletini, na Electronic Engineer from UNLP, went to TIMA in june for a six months period
- Marcelo works with Dr Eitel Peltzer in modelling radiation effects on electronic semiconductor devices at UNLP

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Research subject at TIMA

- *Study and implementation of hardware and software tools for radiation test of a complex processor to be used in space applications*

Objectives:

Study and adaptation of existing hardware tools (THESIC) to the chosen target

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Chosen target

The main features of the MIPS TX49/H2 de Toshiba are:

- **High performannce, RISC based 64 bits architecture**
- **64 GB of physical memory space**
- **Optimized with five levels of pipeline**
- **Hamming Code using EDAC function (Error Detection And Correction), what makes it interesting for these studies**

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Tasks forseen

- Program the Toshiba processor MIPS TX49/H2 with a chosen strategy to inject radiation faults and study errors due to Dingle Event Effects (SEE)
- Build an interface between the processor and Tester in Verilog, to be ported afterwords to an FPGA. That interface allows the connexion between the signals to be measured on the target and the THESIC platform
- Depending on time constrains, perform the injection and further measurements to check the results with theroretical work. The radiation tests are scheduled for the end of 2004.

July 10, 2004

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