LoRelei - Low-energy and Reliable reconfigurable processing systems

Marie Curie Actions - Project No: 295231

Report on the mobility of Anderson Luiz Sartor to TU Delft

Anderson Luiz Sartor met the faculty members within the Computer Engineering group and other selected researchers within the Computer Science and Engineering departments, all within the Faculty of Electrical Engineering, Mathematics and Computer Science. In addition, his advisor, Antonio Carlos Schneider Beck, was in Delft by the time of arrival, working on topics related to the LoRelei project. He was assigned an office and Internet access.

The main goal of his stay at TUD was to:

- Propose and implement fault tolerance techniques for the ρ-VEX processor and work with TUD researchers on the topics which are the subject of joint cooperation.

The first point was addressed with many face-to-face meetings with the researchers within the Computer Science and Engineering department and they focused on several topics:

- Fault tolerance applied to the ρ-VEX processor: This work fits within WP1 (“FPGA-based systems”). It was proposed and implemented three mechanisms to provide fault tolerance for the ρ-VEX processor. The first is a Dual Modular Redundancy (DMR) with an instruction rollback mechanism that allows the detection and correction of errors with low overhead. The second exploits idle phases within the program to apply a selective duplication to the instructions. Finally, the third duplicates the instructions adaptively by exploiting idle slots within the instruction bundle. In addition, it was implemented a configurable threshold that allows the fault tolerance to be tuned, reducing the instruction-level parallelism of the application when more fault tolerance is needed. Therefore, providing a trade-off between fault tolerance and performance. This work led to the following publication: SARTOR, ANDERSON L. ; LORENZON, ARTHUR F. ; CARRO, LUIGI ; KASTENSMDT, FERNANDA ; WONG, STEPHAN ; BECK, ANTONIO C. S. A Novel Phase-Based Low Overhead Fault Tolerance Approach for VLIW Processors. In: 2015 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2015, Montpellier. p. 485-490. In addition, more papers are under review.

- Run-time phase prediction for the ρ-VEX processor: This work fits within WP1 (“FPGA-based systems”), it was developed with TUD researchers and led to the following publication: GUO, Q. ; SARTOR, A. L. ; BRANDON, A. ; BECK, A. C. ; ZHOU, X. ; WONG, S. . Run-time Phase Prediction for a Reconfigurable VLIW Processor. In: Design, Automation and Test in Europe Conference and Exhibition (DATE), 2015, Dresden, Germany.

- Evaluation of energy savings on the ρ-VEX processor through dynamic issue-width adaptation: This work fits within WP1 (“FPGA-based systems”), it was developed with TUD researchers and led to the following publication: GIRALDO, J. S. P. ; SARTOR, A. L. ; CARRO, L. ; WONG, S. ; BECK, A. C . Evaluation of Energy Savings on a VLIW Processor through Dynamic Issue-width Adaptation. In: IEEE
International Symposium on Rapid System Prototyping (RSP), 2015, Amsterdam, The Netherlands.

- Sparse VLIW instruction encoding scheme compatible with generic binaries for the p-VEX processor: This work fits within WP1 (“FPGA-based systems”), it was developed with TUD researchers and led to the following publication: BRANDON, A.; HOOZEMANS, J.; STRATEN, J. V.; LORENZON, A. F.; SARTOR, A. L.; BECK, A. C.; WONG, S. A Sparse VLIW Instruction Encoding Scheme Compatible with Generic Binaries. In: International Conference on Reconfigurable Computing and FPGAs (ReConFig), 2015, Mayan Riviera, Mexico.