Identification and Classification of the Effects of SEUs in the Configuration Memory of SRAM-based FPGAs

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Partners

- CAD Group, Politecnico di Torino
- DEI, Università di Padova
- INFN-LNL, Sezione di Padova.
Goal

- Identify the most sensitive regions of SRAM-based FPGAs
- Evaluate the effects of SEUs in the FPGA configuration memory.

Outline

- Motivation
- Adopted Methodology
- Experimental Set-up
- On-going work.
FPGA architecture

- Composed of:
  - Configuration memory
  - Programmable logic (CLB)
  - Interconnection network (routing)

SEUs into the configuration memory

- May produce modifications to:
  - LUT resources
  - CLB internal network
  - Routing through CLBs.
Approach

- Radiation Testing
- Simulation-based Fault Injection.

Benchmark FPGA architecture

- **Virtex XCV300PQ240-4:**
  - based on a SRAM configuration memory
  - 32x48 CLB matrix
  - almost 7,000 equivalent logic cells
  - 320,000 system gates
  - 64 Kbit of embedded RAM.
Radiation testing

- Radiation experiments carried out at the Tandem Van De Graaff Accelerator of INFN, Legnaro (PD), Italy
- Various ions types from Carbon to Iodine featuring LET values between 1.6 and 62 MeV·cm²/mg used.

Experimental Set Up

- PowerPC-based (MPC860) control host
- A second Virtex FPGA used as reference for the DUT.
Stimulation and Observation

- The DUT is continuously stimulated by a given set of inputs vectors, and the corresponding outputs are observed.
- As soon as a mismatch on the output values is observed between the expected values and the read ones the test is stopped and the configuration read back.

Obtained results: cross section

```
<table>
<thead>
<tr>
<th>LET [MeV cm^2 / mg]</th>
<th>Device Cross Section per bit [cm^2/bit]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.00E-11</td>
</tr>
<tr>
<td>2</td>
<td>1.00E-10</td>
</tr>
<tr>
<td>4</td>
<td>1.00E-09</td>
</tr>
<tr>
<td>6</td>
<td>1.00E-08</td>
</tr>
<tr>
<td>8</td>
<td>1.00E-07</td>
</tr>
<tr>
<td>10</td>
<td>1.00E-06</td>
</tr>
<tr>
<td>12</td>
<td>1.00E-05</td>
</tr>
</tbody>
</table>
```
Modeling SEU effects

- Goal:
  - To develop an environment to analyze SEU effects in FPGA-based designs early in the design phase:
    - Fault models
    - Fault simulator.

Fault model definition

- The configurations recorded during radiation testing are analyzed to identify SEU effects on the FPGA resources
- Manual inspection of SEU effects in the device configuration files:
  - Reverse engineering of device configuration
  - Identification of faulty scenario.
On-going work

- Identification of faulty scenario almost completed
- Synthesis of suitable fault models
- Implementation of fault simulation algorithms.