Does Placement Affect SEU Sensitivity of SRAM-based FPGAs?

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Abstract—The paper investigates the influence of the placement on the SEU sensitivity of designs implemented in SRAM-based FPGAs. The experimental evaluation of an FFT sample design has been accomplished by the FLIPPER and STAR tools.

Index Terms—Placement, Field Programmable Gate Arrays (FPGA), Single Event Effects, Fault Injection.

I. INTRODUCTION

Today’s applications witness an ever increasing use of SRAM-based Field Programmable Gate Arrays (FPGA). Their reduced development costs complement the well-known features of high gate density, performances, and flexibility enabling solutions in a highly performing and cost effective way.

In space and avionic applications the adoption of SRAM-based FPGAs (SRAM-FPGA) is challenged by occurrence of radiation-induced upsets, which mandate the adoption of mitigation techniques. Indeed, in case devices whose configuration or user memory is not radiation-hardened, ionizing particles might alter the memory the FPGAs embed affecting the behavior of implemented designs [1], [2].

As far as non radiation-hardened devices are considered, the most challenging effect consists in upsets in the configuration memory, being the largest among the memories the FPGA embeds, and thus the most probable location for upsets. In SRAM-FPGAs the majority of the configuration memory rules the interconnection setting [3]. In case of complex designs showing very dense routing that makes heavy use of the available resources, it is expected that the placement and routing play a significant role in determining the SEU sensitivity of the implemented design. Assuming an FPGA whose routing interconnection is based on switch matrices, such as in the Xilinx case, the density of interconnection into these elements seems to be a critical point. The higher the interconnection density (i.e., the higher the number of interconnection segments implemented by the same switch matrix) the higher the probability that an upset into a configuration bit controlling the switch matrix affects the implemented design.

The main contribution of the present paper is the analysis of the influence of placement of unmitigated circuits on the SEU sensitivity of the configuration memory of SRAM-based FPGAs.

For space or avionic applications characterized by a low upset rate, ad hoc mitigation techniques exploiting optimal placements might be used in order to reduce the application cross section without turning to standard techniques, like Triple Modular Redundancy (TMR) or other.

This paper experimentally investigates these aspects by using the FLIPPER fault injection tool, and the STAR static analysis tool applied on a sample design. FLIPPER is a tool developed for the European Space Agency aimed at evaluating SEU effects in SRAM-FPGAs by fault injection [4], [5]. STAR is able to identify critical bits of the implemented design by performing a static analysis of the circuit that does not take into account the dependency of the error cross section on the workload [6]. A bit is defined as critical if produces a modification of circuit outputs when it is upset.

FLIPPER was used to measure the degree of robustness of selected mitigation techniques [7], while a comparative study with the analytic STAR tool was performed in [8].

The paper is organized as follows. The related works are briefly reported in Section II. The experimental apparatus and procedure with the sample design are described in Section III. The results and analysis are presented in Section IV, while conclusions are finally drawn in Section V.

II. RELATED WORKS

It is known that the placement of a design implemented in SRAM-based FPGA affects somehow its SEU sensitivity. In an early work by Wirthlin et al. [9], the authors reported about fault injection experiments of an 8-bit counter with three different placements in an XC7V2800 device: i) on the left-side close to the IO blocks of the device, ii) on the bottom right corner slightly offset from the IO blocks, iii) in the center of the chip near the top. The adopted simulator [10] showed a 100% increase in SEU configuration bit sensitivity of the last placement with respect to the first one, due to increased routing.

Various works have been published in the literature concerning interconnections estimate, metric, and congestion of FPGA [11]–[13]. Less data are available on the SEU vulnerability of FPGA interconnections.

Careful placement and routing can reduce the SEU incidence of designs implemented in SRAM-FPGAs. Different tools have been developed to this purpose. The reliability-oriented place and route algorithm RoRA is able to minimize the effects of SEUs affecting designs implemented in SRAM-based FPGAs [14]. When coupled to TMR, it enables re-
routing of design in order to avoid criticalities that might impair TMR. An SEU aware placement and routing algorithm for SRAM-FPGA has been proposed in [15]. Results show the SEU rate of implemented circuits can be decreased by placement and routing of about 18% and 12%, respectively, yet with up to 5%-8% increase of critical path delay and power consumption of circuits.

Exploiting unused resources for partial redundancy in SRAM-based FPGAs and the system failure rate property of nets is the idea of the authors in [16]. The method adaptively packs, places and routes circuits to system failure rate due to soft errors, based on redundancy made from remained free resources. Results show that if the maximum tolerable overall overhead (area, timing, and power) is 20%, failure rate decreases up to 13%.

III. TEST APPARATUS AND PROCEDURES

FLIPPER was conceived to emulate bit-flip faults within the configuration memory of SRAM-FPGAs. The fault model adopted in FLIPPER is the bit-flip of configuration memory cells [5]. Various Experimental activities were accomplished by using the FLIPPER platform [5], [7], [8], [17].

In this work FLIPPER has been exploited for investigating the consequence of a single bit-flip injection over a high number of trials. A statistical measure of design robustness against the single bit-flip in the configuration memory is obtained by collecting the number of functional faults across a high number of injection runs.

The sample design consists of five copies of an FFT (Fast Fourier Transform) module. Serial inputs and outputs are used in all modules. The five FFT modules work independently of each other, clock and reset nets being the only common resources.

Each FFT instance performs a Fourier Transform on a data matrix. The data, stored in the matrix, are generated by randomized input data. A signature of the computed transform is then shifted out to the serial output of the module.

Five design variants have been analyzed by means of injection campaigns. The variants differ for the applied placement constraints. In particular, we used four different constraints in terms of available area (P1, P2, P3, P4) and one specific placements (P5). In the first four variants the available design area is progressively reduced, while in P5 the placement in the central area is inhibited. Fig. 1 shows the five variants.

Table I Resource utilization for the implemented circuits

<table>
<thead>
<tr>
<th>Variant</th>
<th>FF</th>
<th>LUT</th>
<th>Slice</th>
<th>IOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>2.66%</td>
<td>28.82%</td>
<td>35.16%</td>
<td>2.79%</td>
</tr>
<tr>
<td>P2</td>
<td>3.61%</td>
<td>39.06%</td>
<td>47.66%</td>
<td>2.79%</td>
</tr>
<tr>
<td>P3</td>
<td>4.73%</td>
<td>51.14%</td>
<td>62.39%</td>
<td>2.79%</td>
</tr>
<tr>
<td>P4</td>
<td>6.69%</td>
<td>72.37%</td>
<td>88.29%</td>
<td>2.79%</td>
</tr>
<tr>
<td>P5</td>
<td>5.55%</td>
<td>60.02%</td>
<td>73.22%</td>
<td>2.79%</td>
</tr>
</tbody>
</table>

Fig. 1. Qualitative schemes for placement constraints of the design variants. The allowed area is in gray.
to investigate the initial guess on the interconnection density, by analyzing the contribution of critical bits in each device resource category. Resource categories are as follow: look up tables (LUT), multiplexers (MUX), configurable logic blocks (CLB), and programmable interconnection points (PIP).

According to STAR, the following types of faults can be distinguished:
- Open: SEUs provoking a disruption of a signal;
- Short: SEUs provoking a short-circuit between two signals;
- Antenna: SEUs that activate a switch to an interconnection which is not used inside the FPGA.

The graph in Fig. 3 reports the number of critical bits for each resource category, normalized with respect to the same category of the P1 version, for the progressively constrained design variants. The result shows that the main contribution to the increase of sensitivity comes from the PIP resources. Furthermore, the graph highlights that only the PIP category has a remarkable and monotonic correlation with slice utilization.

In particular, as shown in Fig. 4, among the interconnection errors only the short and the open categories increase with the slice utilization. Moreover, the short errors increase more than open errors with the slice utilization. This confirms the initial guess about the interconnection density.

In order to compare the experimental results obtained from FLIPPER with the static analysis results given by STAR, it is worth pointing out that the "antenna" errors just add a parasitic element, which could increase propagation delay or collect disturbances, but they do not affect the Boolean function performed by the FPGA.

Fig. 5 shows the increase of short and open errors (normalized with respect to errors of the P1 version) with the slice utilization. The results in Fig. 5 and in Fig. 2 are very similar, and demonstrate that the SEU sensitivity increases with the increase of the slice utilization.

The unconstrained placement (P1) has the lowest number of critical bits, and therefore the lowest number of functional faults. Any constraint in the placement increases the use of the interconnection resources, leading to an increase in both short and open errors.

Indeed, by forcing the design to be placed in progressively reduced areas, we can expect that a higher number of PIPs belonging to the same switch matrix are used to implement the circuit. As a result, an upset affecting the configuration memory of a switch matrix in a tightly-packed design is more likely to create short circuits among PIPs than in a less tightly-packed design.

V. CONCLUSION

The experimental results reported in the paper suggest that the slice utilization is an interesting parameter for comparing...
different placements with respect to their SEU sensitivity, due to the correlation between slice utilization and the interconnection density. Results also suggest that placement constraints should be reduced in radiation-tolerant designs, as they increase the use of routing resources and the number of critical bits.

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REFERENCES